PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G11B 7/125, 19/04, 11/105, H01S 3/13 — A1

(11) International Publication Number: **WO 00/39793**

(43) International Publication Date: 6 July 2000 (06.07.00)

(21) International Application Number: PCT/EP99/10067

(22) International Filing Date: 14 December 1999 (14.12.99)

(30) Priority Data:
98204434.9 24 December 1998 (24.12.98) EP

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 5621 BA Eindhoven (NL).

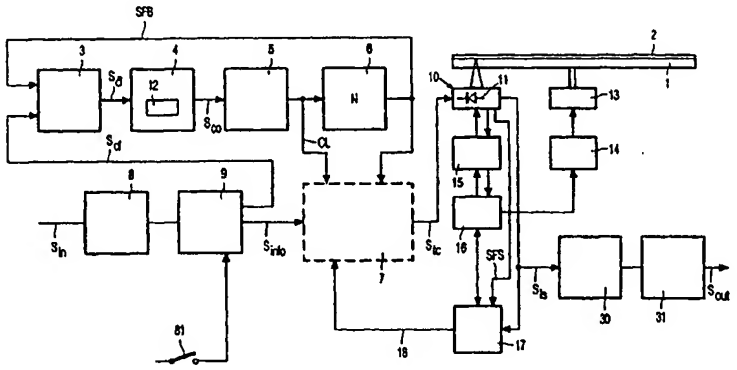
(72) Inventors: IMMINK, Albert, H., J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). DIJKMANS, Eise, C.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). VAN DEN HOMBERG, Johannes, A., T., M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DE JONG, Durk, J.; Internationaal Octroibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States: CN, JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: OPTICAL RECORDING/REPRODUCING DEVICE HAVING A SYSTEM FOR THE REDUCTION OF LASER NOISE WHEN READING DATA FROM THE RECORD CARRIER



(57) Abstract

The device described has a first operational state for writing information onto a record carrier (1) and a second operational state for reading information from a record carrier (1). The device comprises a phase-locked loop (3-6) for generating a clock signal (CL) from a reference signal (SCL). The device further comprises a control unit (7) for generating a pulsed transducer control signal (Str) in response to an information signal (Sinfo) and the clock signal (CL). The device also comprises a transducer (10) for generating physically detectable patterns in the record carrier (1) in response to the transducer control signal (Str). The device also comprises a transducer (10) for generating a read signal (Sls) in response to physically detectable patterns in the record carrier (1) in the second operational state. The transducer (10) for generating the read signal (Sls) comprises a radiation source (11). The device further comprises a power supply (7) which supplies the radiation source (11) with an electric power. The phase-locked loop (3-6) comprises memory means (12) for memorizing, in the first operational state, a memory value which is a measure of the supplied clock signal (CL). In the second operational state, the phase-locked loop (3-6) generates the clock signal (CL) in response to the memorized memory value and causes a high-frequency modulation in the electric power supplied by the power supply (7).

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

OPTICAL RECORDING/REPRODUCING DEVICE HAVING A SYSTEM FOR THE REDUCTION OF LASER NOISE WHEN READING DATA FROM THE RECORD CARRIER

The invention relates to a device having a first operational state for writing information onto a record carrier, comprising

- a phase-locked loop for generating, in the first operational state, a clock signal from a reference signal,
- a control unit for generating, in the first operational state, a pulsed transducer control signal in response to an information signal and the clock signal,
- a transducer for generating, in the first operational state, physically detectable patterns in the record carrier in response to the transducer control signal.

A device of this type is known from USP 5,126,985. The device is suitable for writing information onto a record carrier of the thermomagnetic type. In the known device, the transducer for generating, in the first operational state, physically detectable patterns in the record carrier comprises an optical write head and a magnetic write head. The device is provided with a synchronizing circuit for generating control signals from the information signal for the optical write head and the magnetic write head. The synchronizing circuit comprises a phase-locked loop which generates a clock signal from the information signal. Here, the pulse -generating means are constituted by a delay unit. The pulsed transducer control signal generated by the pulse-generating means is constituted by the clock signal delayed in the delay unit. This transducer control signal is a response to the clock signal and the information signal. The feedback signal-generating means for generating a feedback signal in response to the clock signal are constituted by a connection between the controllable oscillator and the error signal-generating means. The error signal-generating means comprise means for generating an instantaneous error signal which is a measure of the instantaneous difference in phase between the information signal and the clock signal which has been fed back. The error signal-generating means also comprise a loop filter generating an error signal from the instantaneous error signal, which is a measure of an average difference in phase between the information signal and the feedback signal. In this case, the control signal-

generating means are constituted by a direct connection between the loop filter and the controllable oscillator. The error signal is used as a control signal.

When optically reading information from a record carrier, a read head provided with a radiation source is usually used. A radiation beam generated by the radiation source is imaged on the record carrier. By detecting radiation reflected by the record carrier, a read signal can be generated which represents the information recorded on the record carrier.

Practice has proved that radiation sources used for these purposes exhibit noise referred to as "relative intensity noise". This is a drawback because this noise also leads to disturbances in the read signal.

It is an object of the invention to provide a device of the type described in the opening paragraph, in which the influence of relative intensity noise when reading a record carrier is limited. According to the invention, the device is therefore characterized by a second operational state for reading information from a record carrier, which device comprises a transducer for generating, in the second operational state, a read signal in response to physically detectable patterns in the record carrier, which transducer for generating the read signal comprises a radiation source, said device also comprising a power supply which supplies the radiation source with an electric power, the phase-locked loop comprising memory means for memorizing, in the first operational state, a memory value which is a measure of the supplied clock signal, while, in the second operational state, the phase-locked loop generates the clock signal in response to the memorized memory value, and, in the second operational state, causes a high-frequency modulation in the electric power supplied by the power supply.

In the device according to the invention, the power with which the radiation source is fed is high-frequency modulated, for example, at a frequency of several hundred MHz, for example, 500 MHz. The inventors have found that this reduces the influence of relative intensity noise. In the device according to the invention, no separate oscillator is necessary for high-frequency modulation of the power for the radiation source. The controllable oscillator, which, in the first operational state, supplies the clock signal for the pulse-generating means, functions in the second operational state as an oscillator for causing the high-frequency modulation.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows diagrammatically a device according to the invention,

Fig. 2 shows a transducer used in the device,

Fig. 2A shows a detail of the transducer, taken on the line IIA-IIA in Fig. 2,

Fig. 3 shows, in greater detail, a control unit of the device of Fig. 1,

Fig. 4 shows diagrammatically the possible contents of a look-up table used in the device,

Fig. 5 shows, in greater detail, a part of the control unit shown in Fig. 3,

Fig. 6 shows a further detail of the detail shown in Fig. 5,

Fig. 7 shows some signals in the device of Fig. 1.

Fig. 1 shows a device having a first operational state for writing information onto a record carrier 1. The record carrier 1 is, for example, of a type which is writable once, for example, a record carrier of the ablative type. Alternatively, the record carrier may be of a type which is rewritable, for example, a record carrier provided with an information layer of a material having an amorphous structure which can be locally converted into a crystalline structure by consecutively heating and cooling the information layer. Such a material is, for example, an alloy of Te, Se and Sb. A survey of such materials is given in "Principles of Optical Disc Systems" by G. Bouwhuis, J. Braat, A. Huyser, J. Pasman, G. van Rosmalen and K. Schouhamer Immink, Adam Hilger Ltd., Bristol 1985, pp. 219-225. Alternatively, the record carrier may be, for example, of the magneto-optical type. These record carriers are provided with an information layer of a magnetizable material. The magnetization is influenced by locally heating the information layer above the Curie temperature, for example, by means of a laser beam and by simultaneously applying a magnetic field. The device shown comprises a phase-locked loop 3-6 for receiving a reference signal SCL in the first operational state and for generating a clock signal CL from the reference signal SCL. In the embodiment shown, the reference signal SCL is also a clock signal, namely a clock signal which is synchronous with the information to be written. The phase-locked loop 3-6 comprises error signal-generating means 3 for generating an error signal Sδ which is a measure of an average difference in phase between the reference signal SCL and a feedback signal SFB. The phase-locked loop 3-6 also comprises control signal-generating means 4 for receiving the error signal

Sδ and generating an oscillator control signal Sco which is dependent on the error signal Sδ. A controllable oscillator 5 supplies the clock signal CL in response to the oscillator control signal Sco. Feedback signal-generating means 6 generate a feedback signal SFB in response to the clock signal CL. In the embodiment shown, the feedback signal-generating means 6 are constituted by a frequency divider.

The device comprises a control unit 7 for generating, in the first operational state, a pulsed transducer control signal in response to an information signal Sinfo and the clock signal CL. The control unit also uses the feedback signal SFB.

The information signal is generated from an input signal Sin. An error correction encoding is applied with the aid of the error correction encoding means 8. From the signal thus obtained, the information signal is subsequently generated by channel encoding with channel encoding means 9. The channel encoding means 9 also generate the reference signal SCL. This is a clock signal which is in phase with the information signal Sinfo. Alternatively, the information signal Sinfo itself may serve as a reference signal for the PLL. The channel encoding means 9 are, for example, EFM or EFM+ channel encoding means.

In the first operational state, a transducer 10 generates physically detectable patterns in the information layer 2 of the record carrier 1 in response to the transducer control signal Str.

The device has a second operational state for reading information from a record carrier 1. The record carrier 1 may be a record carrier which is written in the first operational state by means of the device but may be alternatively a record carrier provided with an information layer in a different way, for example, in a different device, for example, a device in which the information layer is obtained by pressing. The device comprises a transducer 10 for generating, in the second operational state, a read signal Sls in response to physically detectable patterns in the record carrier. The transducer 10 for generating the read signal comprises a radiation source 11. The device also comprises a power supply, here constituted by the control unit 7, which supplies the radiation source with an electric power. The control signal-generating means 4 comprise memory means 12 for memorizing, in the first operational state, a memory value which is dependent on the error signal Sδ. In the second operational state, the control signal-generating means 4 generate the oscillator control signal Sco in response to the memorized memory value. In the second operational state, the phase-locked loop causes, by means of its output signal So, a high-frequency modulation in the electric power supplied by the power supply 7.

In the embodiment shown, the device is intended for reading and writing information from/onto a disc-shaped record carrier 1. To this end, the device has a motor 13 for rotating the record carrier 1, and a drive unit 14 for driving the motor 13. The radial position of the transducer 10 is determined by a servosystem 15. The servosystem 15 and the drive unit 14 are controlled by a microprocessor 16. The motor 13, the drive unit 14, the servosystem 15 and the microprocessor 16 are of a conventional type. The device also comprises a control unit 17 controlled by the microprocessor 16. The control unit 17 receives signals SFS, SIs from one or more sensors and, in response thereto, adapts parameters of the control unit 7 via a serial bus 18. With these parameters, the supplied radiation power of the radiation source 11 is not influenced by ageing and/or heating of the radiation source 11. Also power supplied to the radiation source 11 may be adapted to the state of the record carrier 1 so that, for example, also in the presence of fingerprints on the record carrier 1, the write signal can be recorded in a reliable manner. In the embodiment shown, the device has a switch 81. A user can operate this switch 81 so that the device assumes either the first or the second operational state. In the second operational state, the value of the information signal Sinfo is maintained until the device again assumes the first operational state.

In the embodiment shown, the transducer 10 is used both for writing information onto the record carrier and for reading information from the record carrier. Alternatively, different transducers may be used for reading and writing information. The transducer 10 is shown in greater detail in Fig. 2. In addition to the radiation source 11, the transducer also comprises an optical system and a first detector 20 and a second detector 21. The optical system is provided with a first beam splitter 22, a lens 23, a second beam splitter 24, a focusing objective 25 and an astigmatic element 26. The second detector 21 is divided into sub-detectors, while at least sub-detectors are arranged on both sides of a line 27 (see Fig. 2A) indicating a direction of a track to be written on a record carrier. In the first operational state, the radiation source 11 generates a radiation beam in response to the control signal Str. The first beam splitter 22 images a fraction of the radiation in the radiation beam on the first detector 20. The output signal SFS supplied by the first detector 20 is applied to the control means 17 for adapting the power supplied to the radiation source 11 to the response of the radiation source 11 to the supplied power. The radiation beam is further imaged on the information layer 2 of the record carrier 1 by the lens 23, via the beam splitter 24 and by means of the focusing objective 25, and this beam causes a physically detectable, in this case an optically detectable effect on this record carrier. In the second operational state of the device, a radiation beam is also generated with the radiation source 11. Similarly as in the first

operational state, the radiation beam is imaged on the information layer 2. Dependent on the optically detectable effect, the information layer 2 reflects a larger or smaller quantity of radiation. The reflected radiation is imaged on the detector 21 via the focusing objective 25, the beam splitter 24 and the astigmatic element 26. In response to the radiation imaged thereon, the detector 21 generates a signal, in this case a fourfold signal. A signal FE, a signal PP and the read signal Sls are derived from the fourfold signal by means of a preprocessor. The signal FE is used by the servosystem 15 for controlling the focus of the radiation beam on the record carrier 1. The signal PP uses the servosystem for the radial positioning of the transducer 10.

An output signal Sout is generated from the read signal by means of error correction decoding means 30 and channel decoding means 31.

The control unit 7 for generating the control signal from the information signal is shown in greater detail in Fig. 3. The control unit 7 comprises a first circuit 40 for generating a resampled information signal Sinfo' which is synchronized with the feedback signal SFB. The first circuit 40 is implemented as a sample-and-hold register which samples the information signal Sinfo upon every pulse of the feedback signal SFB and retains the sampled value until the next pulse of the feedback signal SFB. In practice, the resampled information signal Sinfo' will be substantially identical to the information signal Sinfo. The resampled information signal Sinfo' is applied to a detection circuit 41 for detecting the duration of a time interval in which the information signal is "high". After termination of said time interval, the circuit generates a first information identification II. The information identification II indicates that the resampled information signal Sinfo' was "high" during said duration. When the resampled information signal Sinfo' is "low", the circuit generates a second information identification II during each period of the feedback signal, which second identification indicates that the resampled information signal Sinfo' was low for 1 period of the feedback signal.

The generated first information identification also comprises an indication of the duration of a time interval preceding the time interval in which the resampled information signal Sinfo' was "low". This has the advantage that, when generating the transducer control signal Str for a given logic value of the resampled information signal Sinfo', the history of the resampled information signal Sinfo' can be taken into account. This is important, for example, for phase change recording. In this type of recording, radiation in the form of a series of radiation pulses having a relatively high intensity is generated at a first logic value. Radiation having a relatively low intensity is generated at a second logic value.

The information identification II cannot be generated until after termination of the time interval of a period in which the resampled information signal Sinfo' is "high". Since the duration of these time intervals varies, a delay, which is dependent on the contents of the resampled information signal Sinfo', is produced in the detection circuit 41. To this end, the detector 41 supplies the information identification II to a FIFO register 42. An address generator 43 can subsequently read the information identification II with a constant delay with respect to the resampled information signal Sinfo' from the FIFO register 42. The address generator 43 generates an address A2 of a location in a look-up table 44. The address generator 43 has a first unit 43A for generating a start address A0 and a second unit 43B for generating a relative address A2. A summing device 43C calculates the generated address A2 as the sum of the start address A0 and the relative address A1.

The look-up table 44 comprises parameters for generating a control signal Str for the transducer 10. The address generator 43 also charges a counter 45 with a count NT which corresponds to the duration of an event. An event is herein understood to mean a period in which the resampled information signal Sinfo' was uninterruptedly "high", or in which the resampled information signal Sinfo' was "low" during a period of the feedback signal SFB, or in which the device is in the second operational state during a period of the feedback signal SFB. The detection means 41 detect that the device is in its second operational state when no changes in the resampled information signal Sinfo' have been observed for a period which is longer than the reference period. The reference period is, for example, 15 cycli of the feedback signal SFB. The counter 45 generates a signal Next which causes the FIFO to supply an information identification II associated with a subsequent event to the address generator 43.

The look-up table 44 comprises, inter alia, information SEL1, SEL2 about the value of a control signal Str to be generated and about the duration TA in which this value must be maintained. An example of a look-up table is shown in Fig. 4.The look-up table 44 also comprises information Smod indicating whether the transducer control signal Str must be modulated or not. The information about the value of the control signal Str is in the form of selection signals SEL1, SEL2 for multiplexers 46, 47. In response to a first selection signal SEL1, a first multiplexer 46 supplies a digital value to a first D/A converter 48. In response to this digital value, the D/A converter supplies a minimal current I1 which is necessary to cause the radiation source 11 of the transducer 10 to be controlled to give a response. The power of the current I1 supplied is also proportional to a first reference value Iref1 stored in a register 50. The first multiplexer selects the digital value for the D/A converter from 4 registers 53A-D with reference to the selection signal SEL1. In response to a second selection signal SEL2, the

second multiplexer 47 supplies a digital value to a second D/A converter 49. In response to the digital value, the second D/A converter 49 supplies a further current I2 which is added to the current I1 supplied by the first D/A converter 48 and is supplied to the radiation source 11 in the transducer 10. The further current I2 is proportional to a second reference value Iref2 stored in a register 51. The duration TA for maintaining a value of the control signal Str is in the form of a count for a counter 54. The counter 54 counts a number of pulses of the clock signal CL corresponding to this count and, after termination, supplies a signal to the second unit 43B of the address generator 43 which causes the relative address A1 and hence the generated address A2 to increase by 1. The registers 50, 51, 52A-52D and 53A-53H are coupled to the control unit 17 via the serial bus 18.

Fig. 5 shows the second D/A converter 49 in greater detail. This converter 49 comprises a decoder 60 which converts the digital value supplied by the second multiplexer 47, here an 8-bit value, into a set of 256 digital signals c1-c256. Each of the signals c1-c256 switches its own current source 61. The second D/A converter 49 also comprises an AND gate 62 having a first input which receives the clock signal CL and a second input which receives the signal Smod, indicating whether the control signal Str must be modulated or not. An output of the AND gate 62 is connected to each current source 61. Furthermore, each current source 61 receives the signal Iref1 from the register 50, representing the reference current.

One of the current sources 61 is shown in greater detail in Fig. 6. The other current sources are identical. The current source 61 comprises a first controlled voltage source 63 which is controlled by the signal Iref2 representing the reference current. In the activated state, a first semiconductor element 64 generates a current which depends on the voltage supplied by the voltage source 63. The first semiconductor element 64 is activated when the semiconductor switches 67, 68 are conducting and the semiconductor switches 65, 66 are non-conducting. The state of the semiconductor switches 67, 68 is determined by the output signal c1 of the decoder 60. The state of the semiconductor switches 65, 67 is determined by the modulation signal mod. When information is being written, the modulation signal mod has such a value that the semiconductor switch 67 is conducting and the semiconductor switch 65 is non-conducting. The state of the semiconductor element 64 is now entirely determined by the semiconductor elements 66, 68 which are controlled by the signal c1. When information is being read, the signal Smod assumes a logic value "1". As a result, the signal mod follows the clock signal CL. Now, the semiconductor switches 65, 67 are alternately rendered conducting and non-conducting at the frequency of the clock signal CL.

The first D/A converter 48 differs from the second D/A converter 49 in that it has no input for Smod. In other respects, the first D/A converter 48 is identical to the second D/A converter 49.

The phase-locked loop 3-6 may be of a conventional type as described in, for example, US 5,410,572. The phase-locked loop described in this patent has memory means in the form of a capacitive element. Another conventional phase-locked loop is described in US 5,028,885. The last-mentioned document describes a phase-locked loop provided with digital memory means. Alternatively, a phase-locked loop of the type described in the simultaneously filed application PHN 17.248 may be used. This application is herein incorporated by reference. The phase-locked loop described in this application has switching means which ensure that, during reception of a valid reference signal, the digital memory means do not form part of the loop constituted by the error signal-generating means, the controllable oscillator and the feedback signal-generating means.

The operation of the device according to the invention is elucidated with reference to Fig. 7. For the description below, it is assumed that the reference signal Scl and hence the feedback signal has a frequency of 69.12 MHz. It is further assumed that the feedback signal-generating means 6 divide the frequency of the clock signal CL by a factor of 8 so that the clock signal CL has a frequency of 552.96 MHz. The vertical broken lines indicate transitions of the feedback signal SFB which is locked by the phase-locked loop 3-6 with the reference signal SCL or which is generated autonomously by the phase-locked loop in the absence of a reference signal SCL. The feedback signal SFB has a period T1. Fig. 7A shows the state signal R/W. Prior to instant t1, the device is in its first operational state in which information is written onto the record carrier 1. After the instant t1, the device assumes the second operational state in which information is read from the record carrier 1.

In the example shown, the resampled information signal Sinfo' is an EFM or EFM+ signal. Such a signal may be "low" for periods between 3 T1 and 11 T1 and "high" also for periods from 3 T1 to 11 T1. When writing the resampled information signal Sinfo' onto the record carrier, a "high" period is registered as a mark with a length corresponding to the duration of the "high" period. A "low" period is registered as an unwritten area between marks and with a length which corresponds to the duration of the "low" period. Generally, the length of a mark is mainly equal to the duration of a "high" period of the information signal multiplied by the write velocity. The length of a mark may therefore be expressed in channel bit lengths, in which one channel bit length corresponds to the duration T1 of a channel bit period, i.e. a period of the feedback signal SFB multiplied by the write velocity. The data is written in an

optical record carrier 1 having an information layer 2. The marks representing the information are written in a track on the information layer 2 by the radiation source 11. The marks are areas of the information layer 2 having an optical characteristic which deviates from that of its surroundings. This provides the possibility of optically reading the marks. The resampled information signal Sinfo' shown in Fig. 7B consecutively has a first "low" period of 3 T1, a first "high" period of 8 T1, a second "low" period of 4 T1 and a second "high" period of 3 T1.

Every period T1 in which the information signal is "low" is detected as such by the detector 41. After the address generator 43 has loaded the information identification II, indicating that the resampled information signal Sinfo' was "low" during 1 cycle of the feedback signal SFB, the first unit 43A of the address generator 43 loads the counter 45 with the duration of the information identified by the information identification II, here 1 cycle of the feedback signal SFB. Moreover, the first unit 43A of the address generator 43 generates an absolute address A0 in the look-up table. Also, the first unit 43A of the address generator 43 initializes the second unit 43B with the signal "reset", generating a relative address A1 at a value 0. The sum of the absolute address A0 and the relative address A1 is the address A2 of a location which corresponds to said information. This address A2, which is denoted by ERASE in the example of Fig. 4, comprises SEL1 = 0, SEL2 = 2, TA = 8, SMOD = 0 as parameters. The value of SEL1 causes the first multiplexer 46 to select the register 52A, and the value of SEL2 causes the second multiplexer 47 to select the register 53C. The values registered in these registers 52A, 53C correspond to an adjustment of the power of the radiation source 11 at a first level of, for example, 1.8 mW required for erasing. This power is maintained during 8 cycli of the clock signal CL. The transducer control signal Str generated by the control unit 7 is shown in Fig. 7C. As stated hereinbefore, a delay having a duration of, for example, 16 cycli of the feedback signal SFB occurs when generating the transducer control signal Str. However, for the sake of clarity, the transducer control signal Str is shown synchronously with the resampled information signal Sinfo' in Fig. 7. After 8 cycli have elapsed, a cycle of the feedback signal SFB has also elapsed. The counter 45 then causes new information identification II to be loaded from the FIFO register 42 in the first unit 43A of the address generator 43, in this case also an identification having a "low" value of the resampled information signal Sinfo' during 1 period of the feedback signal SFB. The power of the radiation source 11 is therefore maintained at the first level for another 8 cycli. This is also the case during the next cycle of the feedback signal SFB. After termination of this cycle, the address generator 43 loads an information identification II of one period in which the resampled information signal Sinfo' had a "high" value during 8 cycli of the feedback signal

SFB. In response thereto, the first unit 43A of the address generator 43 loads the counter 45 with the value 8 and generates an absolute address A0 which is the start address of a series of locations in the look-up table 44 which comprises the parameters corresponding to this information. Since the second unit 43B generating the relative address A1 is initialized at 0, the instantaneous address A2 is initially equal to the absolute address A0. This address A0 is denoted by WRITE8*T1 in Fig. 4. The location with this address comprises the parameters SEL1 = 0, SEL2 = 2, TA = 6, SMOD = 0. At these parameters, the power of the radiation source is maintained during the period TA of 6 cycli of the clock signal CL at the first level required for erasing. The counting value TA = 6 is loaded into the counter 54. The counter 54 counts a number of cycli of the clock signal CL corresponding to this counting value and then supplies a signal A+ to the second unit 43B constituted by the relative address generator. Upon reception of this signal A+, the relative address generator 43B raises the relative address by 1. The instantaneous address A2 then indicates a location with the parameters SEL1 = 0, SEL2 = 3, TA = 4 and SMOD = 0. The first and the second multiplexer 46, 47 now choose their input signal from registers 52A and 53D, respectively. The power of the radiation source 11 increases to a second level of, for example, 7.5 mW required for writing a mark. After termination of the period of 4 cycli of the clock signal CL, the counter 54 causes the relative address generator 43B to raise the address A1 again so that now an instantaneous address is selected with the parameters SEL1 = 0, SEL2 = 0, TA = 4 and SMOD = 0. At these parameters, the power of the radiation source 11 is maintained for 4 clock cycli at a third level of, for example, 0 mW. Subsequently, the power of the radiation source 11 is again raised to the second level. Then the power is changed another five times between the second and the third level. Subsequently, a location of the look-up table 44 has been reached with the parameters SEL1 = 0, SEL2 = 1, TA = 6 and SMOD = 0. These parameters represent an adjustment of the power of the radiation source 11 at a fourth level of, for example, 0.5 mW, intended for cooling the information layer 2.

If the detector 41 detects a period in which the resampled information signal Sinfo' has remained unchanged for a period of 15*T1, the state signal R/W assumes a value of 0. During every cycle of the feedback signal SFB when this state is maintained, the detector 41 supplies an information identification II which indicates this. In response thereto, the address generator 43 generates an address A2 which is denoted by "READ" in Fig. 4 and comprises the parameters SEL1 = 0, SEL2 = 2, TA = 8 and SMOD = 1. It is thereby ensured that the power of the radiation source 11 is adjusted at a fifth level of, for example, 0.5 mW, intended for reading. Since SMOD now has the logic value 1, the modulation signal MOD is now equal

to the clock signal CL. As a result, the second D/A converter 49 is switched on and off at the frequency of the clock signal, here 552.96 MHz. The current Str supplied to the radiation source 11 is thereby modulated between a minimal value MIN and a maximal value MAX. The minimal value MIN is the current supplied by the first multiplexer 46. The maximal value MAX is the current which is jointly supplied by the D/A converters in the switched-on state of the second D/A converter. This is shown in greater detail in Fig. 7D. The time scale in this Figure has a resolution which is 8 times higher than in Fig. 7C. It has been found that such a modulation strongly reduces the occurrence of relative intensity noise in semiconductor radiation sources. Instead of generating the modulation signal MOD directly from the clock signal CL, the modulation signal could also be obtained from the clock signal CL via an additional frequency divider. In the embodiment shown, the frequency of the clock signal CL is, however, very suitable for modulating the radiation source 11.

The invention is not limited to the embodiment described. Many variations within the scope of the appendant claims can be conceived by those skilled in the art. In another embodiment, the device is intended for reading and writing information from/onto a record carrier of a different shape, for example, a tape-shaped record carrier. The invention also relates to each and every novel characteristic feature and each and every novel combination of characteristic features.

CLAIMS:

1. A device having a first operational state for writing information onto a record carrier (1), comprising

- a phase-locked loop (3-6) for generating, in the first operational state, a clock signal (CL) from a reference signal (SCL),
- a control unit (7) for generating, in the first operational state, a pulsed transducer control signal (Str) in response to an information signal (Sinfo) and the clock signal (CL),
- a transducer (10) for generating, in the first operational state, physically detectable patterns in the record carrier (1) in response to the transducer control signal (Str),

characterized in that

the device has a second operational state for reading information from a record carrier (1), which device comprises a transducer (10) for generating, in the second operational state, a read signal (Sls) in response to physically detectable patterns in the record carrier (1), which transducer (10) for generating the read signal comprises a radiation source (11), said device also comprising a power supply (7) which supplies the radiation source (11) with an electric power, the phase-locked loop comprising memory means (12) for memorizing, in the first operational state, a memory value which is a measure of the supplied clock signal (CL), while, in the second operational state, the phase-locked loop generates the clock signal (CL) in response to the memorized memory value, and, in the second operational state, causes a high-frequency modulation in the electric power supplied by the power supply (7).

2. A device as claimed in claim 1, characterized in that the device has a common transducer (10) for reading and writing information from/onto the record carrier (1), and in that the control unit (7) is used as a power supply for the radiation source (11) during the second operational state.

3. A device as claimed in claim 2, characterized in that the control unit comprises means (41) for detecting the duration of a time interval in which the information signal (Sinfo)

has a constant logic value, and for generating a signal (II) which comprises an indication of the duration.

4. A device as claimed in claim 3, characterized in that the signal (II) supplied by said means (41) also comprises an indication of the duration of a time interval, preceding the time interval, in which the information signal (Sinfo) has a different logic value.

5. A device as claimed in claim 1, characterized in that the control unit comprises means (40) for resampling the information signal (Sinfo) synchronously with the feedback signal (SFB).

6. A device as claimed in claim 1, characterized in that the device also comprises error correction encoding means (8) and/or channel encoding means (9) for generating the information signal (Sinfo) from an input signal (Sin) by means of error correction encoding and/or channel encoding.

7. A device as claimed in claim 1, characterized in that the device also comprises error correction decoding means (31) and/or channel decoding means (30) for generating an output signal (Sout) from a read signal (Sls) by means of error correction decoding and/or channel decoding.

8. A device as claimed in claim 1, characterized in that the device also comprises a control unit (17) which receives signals (SFS, Sls) from at least a sensor (20) for a radiation power of radiation generated by the radiation source (11), or a sensor (21) for measuring radiation reflected by the record carrier (1), said control unit (18) adapting the radiation power to the received one or more signals.

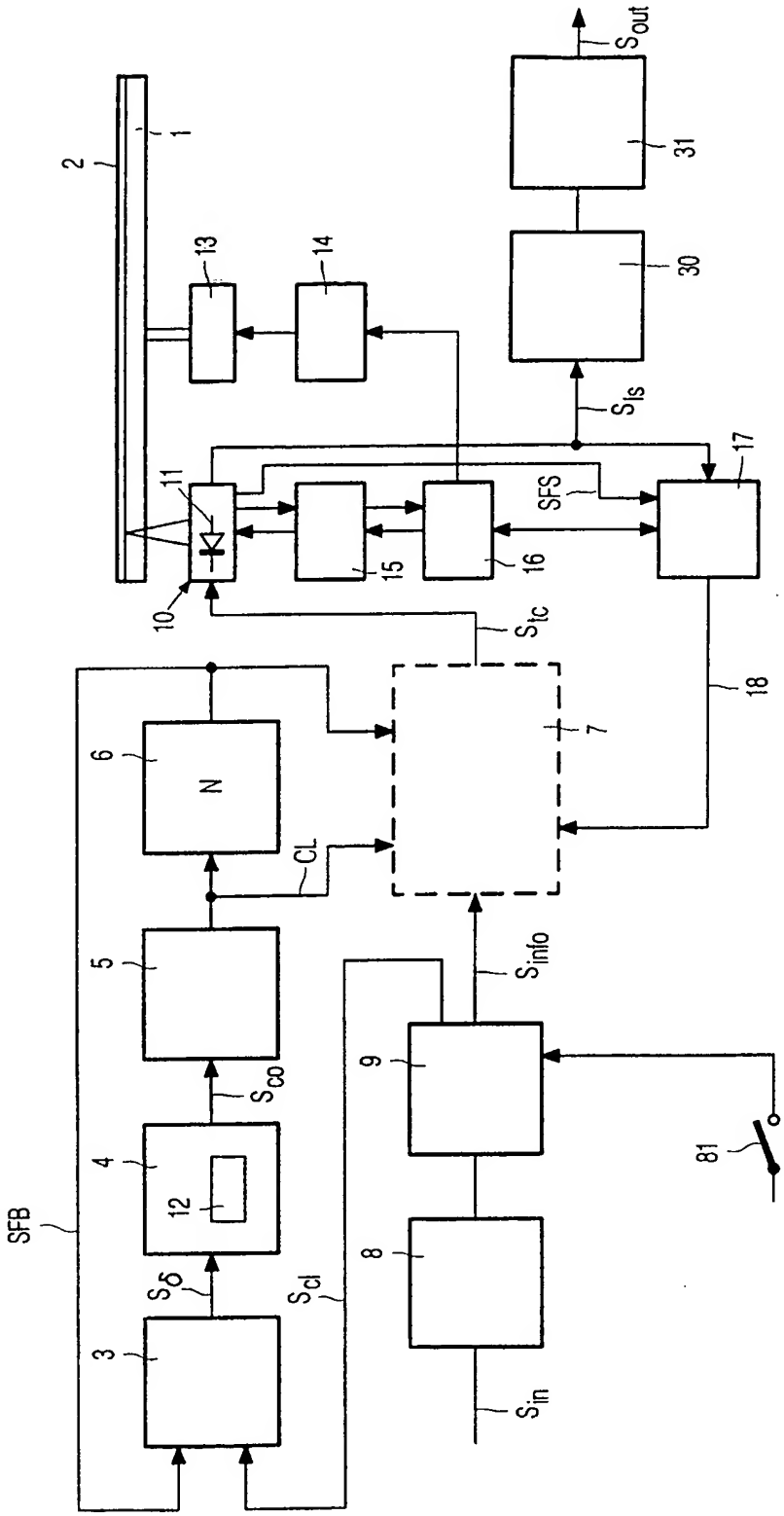

S_{out}
31
30
S_{ls}
17
SFS
11
13
14
15
16
10
S_{tc}
18
7
6
N
CL
5
S_{info}
S_{co}
9
4
12
81
SFB
8
S_{δ}
S_{cl}
3
S_{in}
1
2

FIG. 1

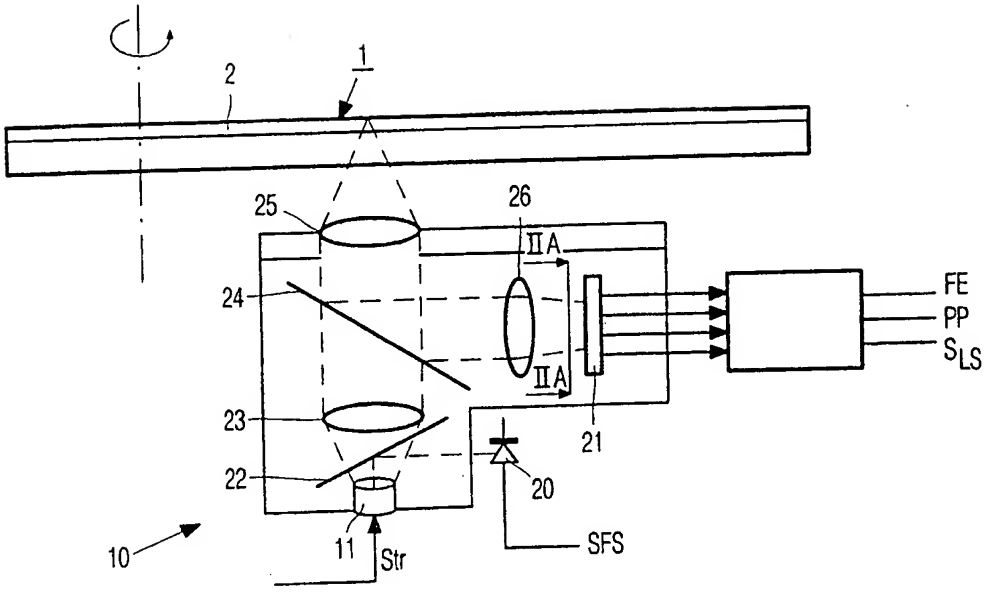

1
2
25
26
IIA
24
IIA
FE
PP
S_{LS}
23
21
22
20
10
11
Str
SFS

FIG. 2

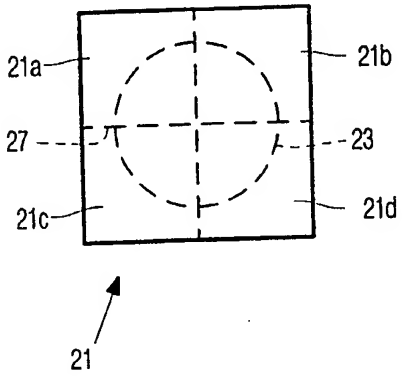

21a
21b
27
23
21c
21d
21

FIG. 2A

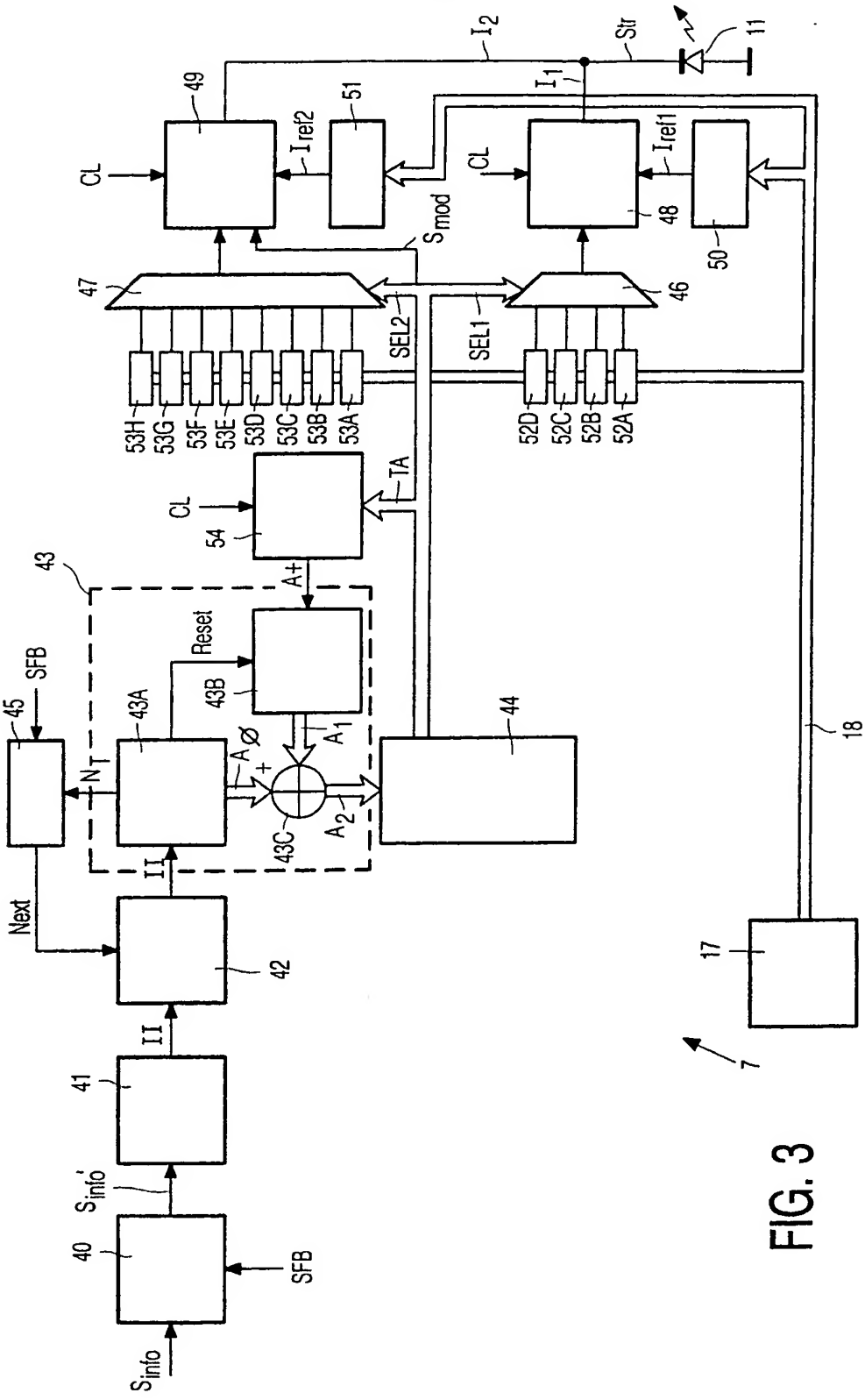

I_2
Str
11
I_1
49
51
I_{ref2}
CL
S_{mod}
CL
I_{ref1}
48
50
47
46
SEL2
SEL1
53H
53G
53F
53E
53D
53C
53B
53A
52D
52C
52B
52A
CL
54
TA
43
A+
Reset
43B
SFB
45
43A
N_T
$A_\varnothing$
A_1
A_2
43C
44
18
II
Next
42
II
41
S_{info}'
40
SFB
S_{info}
17
7

FIG. 3

	SEL1	SEL2	T_A	S_{MOD}
WRITE 3*TI	0	2	6	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	1	6	0
WRITE 4*TI	0	2	6	0
WRITE 8*TI	0	2	6	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	0	4	0
	0	3	4	0
	0	1	6	0
ERASE	0	2	8	0
READ	0	1	8	1

FIG. 4

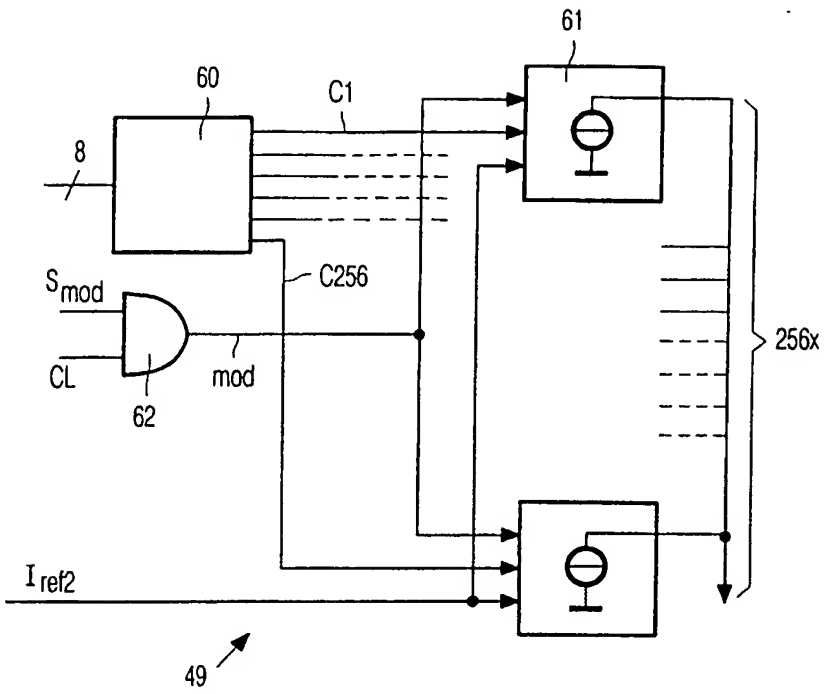

61
60
C1
8
C256
S_{mod}
CL
62
mod
256x
I_{ref2}
49

FIG. 5

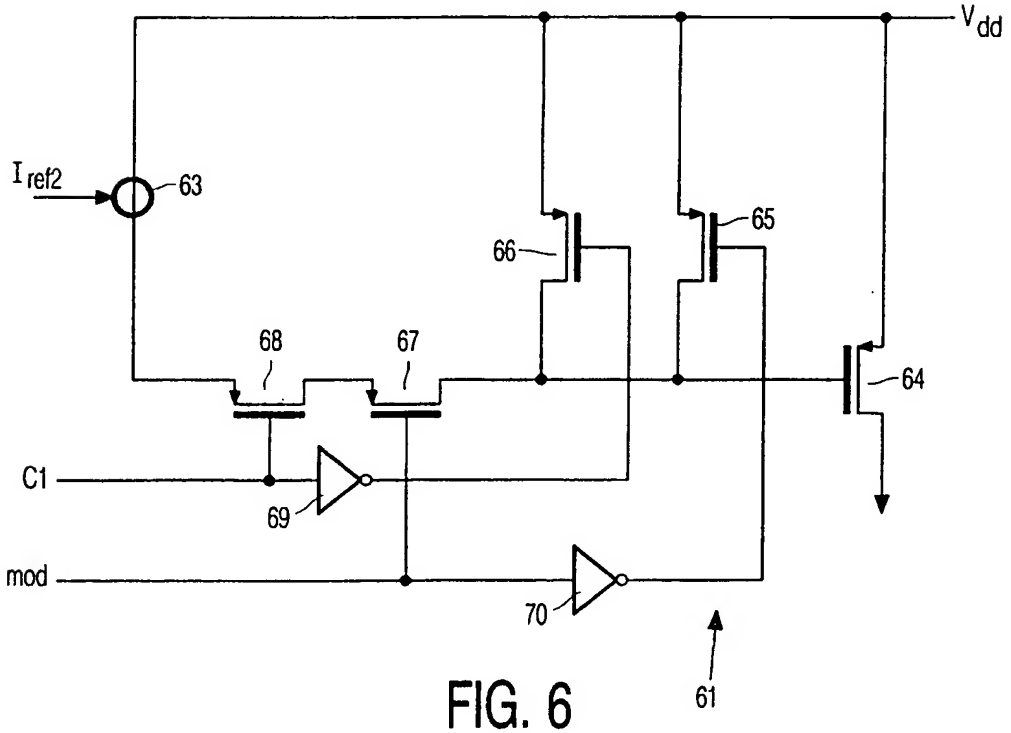

V_{dd}
I_{ref2}
63
66
65
68
67
64
C1
69
mod
70
61

FIG. 6

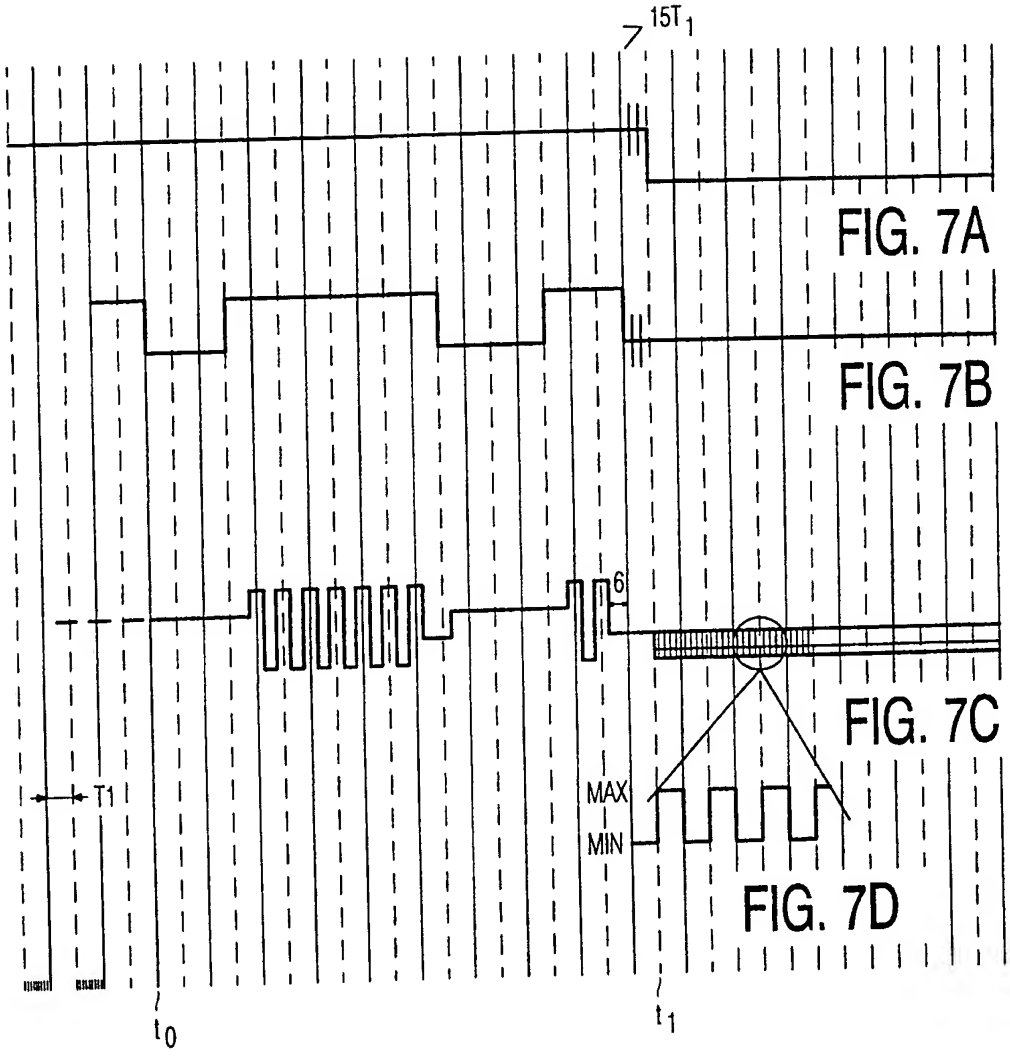


FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/EP 99/10067

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11B7/125 G11B19/04 G11B11/105 H01S3/13

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11B H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 120 389 A (HITACHI LTD) 3 October 1984 (1984-10-03) the whole document	1,2
Y	US 5 126 985 A (SPRUIT JOHANNES H M ET AL) 30 June 1992 (1992-06-30) cited in the application the whole document	1,2
A	US 4 480 325 A (AIKI KUNIO ET AL) 30 October 1984 (1984-10-30)	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 April 2000	26/04/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Benfield, A

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. nal Application No
PCT/EP 99/10067

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0120389 A	03-10-1984	JP 5078093 B	28-10-1993
		JP 59171037 A	27-09-1984
		KR 9103217 B	22-05-1991
		US 4712218 A	08-12-1987
US 5126985 A	30-06-1992	NL 8703011 A	03-07-1989
		AT 94303 T	15-09-1993
		BR 8806542 A	22-08-1989
		CN 1034820 A	16-08-1989
		DE 3883939 D	14-10-1993
		DE 3883939 T	24-03-1994
		EP 0321027 A	21-06-1989
		ES 2045093 T	16-01-1994
		HK 85396 A	24-05-1996
		JP 1208751 A	22-08-1989
		JP 2847117 B	13-01-1999
US 4480325 A	30-10-1984	DE 3027318 A	22-01-1981
		NL 8004159 A	22-01-1981